CLAIMS

We claim:

1. A clock distribution circuit, comprising:

a first clock circuit that is configured to generate a first clock signal responsive to an error signal;

a second clock circuit that is configured to generate a second clock signal responsive to the error signal; and

a phase detector circuit that connects the first clock circuit to the second clock circuit and is configured to generate the error signal responsive to the first and the second clock signals.

2. The clock distribution circuit of Claim 1, wherein the error signal is a first error signal, and wherein the phase detector is a first phase detector, the clock distribution circuit further comprising:

a third clock circuit that is configured to generate a third clock signal responsive to a second error signal; and

a second phase detector circuit that connects the first clock circuit to the third clock circuit and is configured to generate the second error signal responsive to the first and the third clock signals;

wherein the first clock circuit is further configured to generate the first clock signal responsive to the first and the second error signals.

3. The clock distribution circuit of Claim 2, wherein the first clock circuit comprises:

a loop filter circuit that is configured to generate a control signal at an output terminal thereof responsive to the first and the second error signals; and

an oscillator that is configured to generate the first clock signal responsive to the control signal.

4. The clock distribution circuit of Claim 3, wherein the first clock circuit further comprises:

a summation circuit that is configured to add the first and the second error signals to generate a composite error signal, the loop filter circuit being configured to generate the control signal responsive to the composite error signal.

5. The clock distribution circuit of Claim 4, wherein the loop filter circuit comprises:

a first amplifier circuit that is responsive to the composite error signal; and

a second amplifier circuit that is responsive to the composite error signal and is connected to the first amplifier circuit at the output terminal.

6. The clock distribution circuit of Claim 1, wherein the phase detector circuit comprises:

a first pulse generator circuit that is configured to generate a first pulse signal responsive to the first clock signal;

a second pulse generator circuit that is configured to generate a second pulse signal responsive to the second clock signal; and

an arbiter circuit that is configured to generate the error signal responsive to the first pulse signal and the second pulse signal.

7. The clock distribution circuit of Claim 1, wherein the first clock circuit, the second clock circuit, and the phase detector circuit are contained in a single integrated circuit chip.

8. A clock distribution circuit, comprising:

a plurality of phase detector circuits;

a plurality of clock circuits, respective ones of the plurality of clock circuits being directly connected to at least one other of the plurality of clock circuits by respective ones of the plurality of phase detector circuits, respective ones of the plurality of phase detector circuits being configured to generate respective ones of a plurality of error signals responsive to respective ones of a plurality of clock signals generated by the respective ones of the plurality of clock circuits that are directly connected thereby, the respective ones of the plurality of clock circuits being configured to generate respective ones of the plurality of clock signals responsive to

respective ones of the plurality of error signals that are generated by the respective ones of the plurality of phase detector circuits that directly connect the respective ones of the plurality of clock circuits to the at least one other of the plurality of clock circuits.

9. The clock distribution circuit of Claim 8, wherein the plurality of clock circuits comprise:

a plurality of loop filter circuits, respective ones of the plurality of loop filter circuits being configured to generate respective ones of a plurality of control signals at respective output terminals thereof responsive to the respective ones of the plurality of error signals that are generated by the respective ones of the plurality of phase detector circuits that directly connect the respective ones of the plurality of clock circuits to the at least one other of the plurality of clock circuits; and

a plurality of oscillator circuits, respective ones of the plurality of oscillator circuits being configured to generate the respective ones of the plurality of clock signals responsive to the respective ones of the plurality of control signals.

10. The clock distribution circuit of Claim 9, wherein the plurality of clock circuits further comprise:

a plurality of summation circuits, respective ones of the plurality of summation circuits being configured to generate a plurality of composite error signals, respective ones of the plurality of composite error signals corresponding to summations of the respective ones of the plurality of error signals that are generated by the respective ones of the plurality of phase detector circuits that directly connect the respective ones of the plurality of clock circuits to the at least one other of the plurality of clock circuits, the respective ones of the plurality of loop filter circuits being configured to generate the respective ones of a plurality of control signals responsive to the respective ones of the plurality of composite error signals.

11. The clock distribution circuit of Claim 10, wherein the plurality of loop filter circuits comprise:

a plurality of first amplifier circuits, respective ones of the plurality of first amplifier circuits being responsive to the respective ones of the composite error signals; and

a plurality of second amplifier circuits, respective ones of the plurality of second amplifier circuits being responsive to the respective ones of the composite error signals, and being connected to the respective ones of the plurality of first amplifier circuits at the respective output terminals.

12. The clock distribution circuit of Claim 8, wherein the plurality of phase detector circuits comprise:

a plurality of first pulse generator circuits, respective ones of the plurality of first pulse generator circuits being configured to generate respective ones of a plurality of first pulse signals responsive to first respective ones of the plurality of clock signals generated by the respective ones of the plurality of clock circuits that are directly connected by the respective ones of the plurality of phase detector circuits;

a plurality of second pulse generator circuits, respective ones of the plurality of second pulse generator circuits being configured to generate respective ones of a plurality of second pulse signals responsive to second respective ones of the plurality of clock signals generated by the respective ones of the plurality of clock circuits that are directly connected by the respective ones of the plurality of phase detector circuits; and

a plurality of arbiter circuits, respective ones of the plurality of arbiter circuits being configured to generate the respective ones of the plurality of error signals responsive to the respective ones of the plurality of first pulse signals and to respective ones of the plurality of second pulse signals.

13. The clock distribution circuit of Claim 8, wherein the plurality of clock circuits and the plurality of phase detector circuits are contained in a single integrated circuit chip.

14. A method for distributing a clock signal, comprising:

generating a first clock signal responsive to an error signal;

generating a second clock signal responsive to the error signal; and

generating the error signal based on a relative phase difference between the first clock signal and the second clock signal.

15. The method of Claim 14, wherein the error signal is a first error signal, the method further comprising:

generating a third clock signal responsive to a second error signal; and

generating the second error signal based on a relative phase difference between the first clock signal and the third clock signal.

16. The method of Claim 15, wherein generating the first clock signal comprises:

generating the first clock signal responsive to the first error signal and the second error signal.

17. The method of Claim 16, wherein generating the first clock signal comprises:

summing the first and the second error signals to generate a composite error signal;

filtering the composite error signal to generate a control signal; and

generating the first clock signal responsive to the control signal.

18. The method of Claim 14, wherein generating the error signal comprises:

generating a first pulse signal responsive to the first clock signal;

generating a second pulse signal responsive to the second clock signal; and

generating the error signal responsive to the first pulse signal and the second pulse signal.

19. A system for distributing a clock signal, comprising:

means for generating a first clock signal responsive to an error signal;

means for generating a second clock signal responsive to the error signal; and

means for generating the error signal based on a relative phase difference between the first clock signal and the second clock signal.

20. The system of Claim 19, wherein the error signal is a first error signal, the system further comprising:

means for generating a third clock signal responsive to a second error signal; and

means for generating the second error signal based on a relative phase difference between the first clock signal and the third clock signal.

21. The system of Claim 20, wherein the means for generating the first clock signal comprises:

means for generating the first clock signal responsive to the first error signal and the second error signal.

22. The system of Claim 21, wherein the means for generating the first clock signal comprises:

means for summing the first and the second error signals to generate a composite error signal;

means for filtering the composite error signal to generate a control signal; and

means for generating the first clock signal responsive to the control signal.

23. The system of Claim 19, wherein the means for generating the error signal comprises:

means for generating a first pulse signal responsive to the first clock signal;

means for generating a second pulse signal responsive to the second clock signal; and

means for generating the error signal responsive to the first pulse signal and the second pulse signal.

24. The system of Claim 19, wherein the means for generating the first clock signal, the means for generating the second clock signal, and the means for generating the first error signal are contained in a single integrated circuit chip.

25. A method of distributing a clock signal over an integrated circuit, comprising:

independently generating a plurality of clock signals on the integrated circuit such that respective ones of the plurality of clock signals are distributed to respective portions of the integrated circuit; and

synchronizing phases of the plurality of clock signals to one another.

26. A system for distributing a clock signal over an integrated circuit, comprising:

means for independently generating a plurality of clock signals on the integrated circuit such that respective ones of the plurality of clock signals are distributed to respective portions of the integrated circuit; and

means for synchronizing phases of the plurality of clock signals to one another.